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EFFICIENT ON-CHIP INTERCONNECTS USING CMS SCHEME WITH VARIATION TOLERANT

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Abstract— ***Current Mode Signaling Scheme-Bias is one of the efficient schemes to achieve high-speed and low power communication over long On-Chip interconnects. In early days the repeaters and boosters circuits [4] are used to drive the on-chip interconnects. In this paper CMS scheme with various types of delay elements which is inserted in the circuit is used to analyze the performance in terms of power and tolerant variation.CMS scheme has an importance that it has a trade-off between speed and power as in[1]. In addition, the voltage swing on the line is reduced in our proposed scheme as in [2]. By the inserting a conventional buffer as delay element the improvement in energy/bit is 87% as in [1].Further to improve the performance of the CMS-Bias the d-latch can be used as a delay element which consumes less power compared to buffer.***

Keywords— Cms Scheme, Interconnects, Process Variation, Signaling Scheme and Variation Tolerant.

I. INTRODUCTION

In VLSI the SoC has take major part of designing a chip where the specifications and requirements are made very accurately. The main objective of the on-chip interconnect network is to made the speed and power consumption in effective way. In the CMOS technology there is a presence of process variation which can be within the die or between the die. Hence the schemes used in the network will withstand the process variation occurring in on-chip interconnects. By referring the literature survey there are many schemes used in on-chip interconnects improve the performance of the system on-chip such as self-timed repeaters, boosters and voltage mode signaling. The powers consumed by the above schemes are more compared to the power consumed by the current mode signaling scheme which is proposed technique. This scheme is more efficient for long wires.

The main advantage of our CMS scheme is due to low voltage swing as in [1] on the line where the noise margin would be reduced in the circuit. Here the discussion is about the variation tolerance in the inter die and intra die for on-chip interconnects. Intra die is nothing but the communication of the systems within the die where the inter die is defined as the communication of the systems between the die.

II. ANALYSIS OF CMS SCHEME

2.1 Weak Driver

The p channel driver gate is low (enabled) when the input is 1.As the line reaches *VDD − VTp*, the upper p channel transistor turns off, restricting line voltage swing. Similarly the n channel driver transistor is enabled when the input is 0 and the lower transistor turns off when the input approaches *VTn* during discharge.

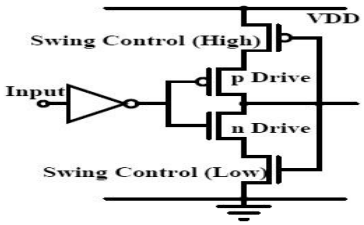

Fig 1: Weak driver

2.2 Strong Driver

The feedback inverter acts as an inverting amplifier converting low swing logic levels on the wire to full swing (inverted) CMOS logic level on its output. P channel gate is low (enabled) only when the input is high AND the line is at 0.N channel gate is high (enabled) only when the input is low AND the line is at 1.Input to the feedback inverter is a low swing level around *VDD*/2. Therefore it consumes static power.

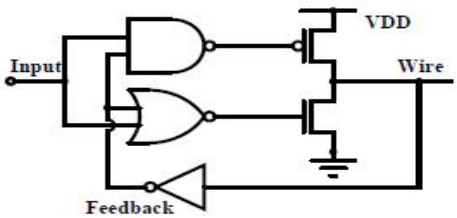

Fig 2: Strong Driver

2.3 Long channel, short channel transistor

A long-channel device will behave according to the square-law model the behavior of a short-channel device will not be accurately predicted by the square-law model. In long channel transistors Channel length L must be much greater than the sum of the drain and source depletion widths. In proposed bias generation circuits variation in short channel MOSFETs is more as compared to long channel MOSFETs.

III. EXISTING SYSTEM

3.1 Performance of nand, nor, inverter amplifier

The proposed transmitter employs two drivers (a strong driver and a weak driver) with NAND and NOR gates .NAND and NOR gate turn on the strong driver for short duration. Inverter amplifier in the receiver and bias circuit in the transmitter consume static power.

3.2 CMS Scheme with driver pre-emphasis

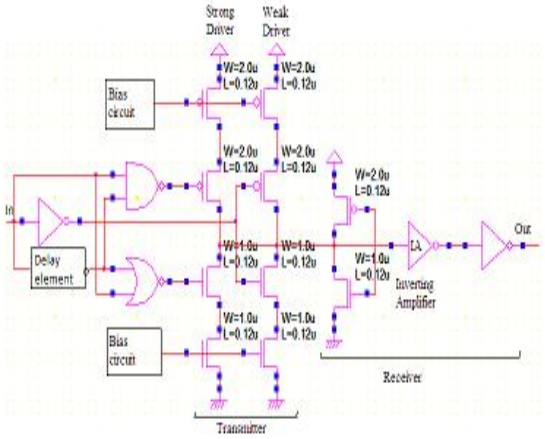

Fig 3: CMS Scheme with Delay Element

Driver Pre-emphasis is the technique of supplying large current/voltage to the line during transitions of input and very small current/voltage in the steady state. This CMS consists of transmitter and receiver. Strong and weak drivers are the part of transmitter. The strong driver is turned off after the line voltage crosses the switching threshold of the feedback inverter. At the receiving end, the line voltage is held near the Vm of the receiver (Vmrx).The steady-state voltage swing on the line is given by the product of the static current supplied by the weak driver and the small signal input impedance of the receiver as in [1]. The inverter following the inverter-amplifier takes the output to CMOS logic levels. In this scheme, the transmitter's strong driver is turned on is controlled by a delay element and not by the feedback. The bias voltage given to the NMOS and PMOS is Vbn and Vbp. The scheme has receiver with diode connected inverter by an inverter chain. The Inverter Amplifier (IA) and the following inverters amplify the small line voltage to digital logic as in [1]. The strong driver is identified by the delay element connection and the weak driver is found by the input inverter.

This scheme is robust against inter-die variations due to the feedback in the transmitter and receiver circuits as long as Vm of the transmitter (Vmtx) and receiver are the same as in [1]. However, Vmtx and Vmrx are different as transmitter receiver is placed far. Consider Vmtx is less than Vmrx. In this case the receiver kept its threshold that is Vmrx which is more than Vmtx. As a result, the strong driver is turned on to pull the line voltage below Vmtx. Once the line voltage is pulled below Vmtx the strong driver is turned off. However, now as the receiver is suppose to hold the line voltage at Vmrx, the line voltage rises to Vmrx which in turn activates strong driver. Like this way voltage on the line swings between Vmtx and Vmrx even though the input is constant logic "0".During 0 to 1 transition in the input, the strong driver is turned off before voltage at the receiver end comes to Vmrx. During 1 to 0 the strong driver is activated after line voltage at the transmitter end comes to Vmrx. From the above lines we can understand that the delay scheme is high for 1 to 0 compared to 0 to 1 transition. If Vmtx>Vmrx, the line voltage is fluctuated when input is constant at logic 1 and 1 to 0 transition is slower than 0 to 1 transition. Anyway the delay will reduce the throughput of the scheme during 0 to 1 and 1 to 0.

3.3 Bias circuit

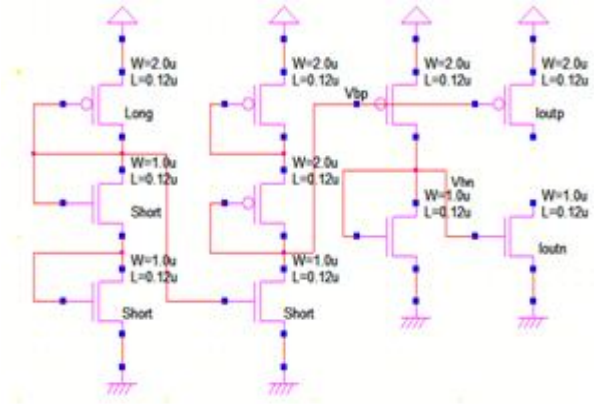

Fig 4: Process corner aware bias circuit

The bias circuit used here is derived from the resistance based circuit where the long channel MOS will act as a resistance

because of the threshold voltage and gain. In the load device the bias circuit variation is high as in [7].

So, that the long channel transistor as load and Short channel can act as a sensor device. Considering an ideal resistance circuit, PMOS bias voltage (Vbpo) increases and decreases from its value that is PMOS becomes fast/slow due to process variation. So, the output of PMOS (Ioutp) does not change much with process variation. Similarly, Vbno changes where the variation is less compared to PMOS. Resistance value can be varied from plus or minus 15%.Finally, the bias voltages for PMOS and NMOS change not due to variations in the PMOS and NMOS transistors. The occurrence is due to the variation in the resistance. In this circuit there is a trade-off between area of a resistor and power consumption. The variation is low in the resistive bias circuit where high in the process corner bias circuit. Because the process variation is more in load device where it is low in sensor device. So that long channel transistor will act as a load and short channel will act as a sensor. Due to the connection of two short channel device in the bias circuit the Vthn and k made very strong where 180-nm technology is used.

IV. SIMULATION ANALYSIS

Here the microwind is chosen as a simulating tool to reduce the design of layout complexity. This microwind consist of Dsch2 and microwind2 where the Dsch2 (Digital schematic) is used to verify the circuit logically whereas the microwind2 has the use of creating a layout for the complex circuits. The Dsch2 provides a hierarchical design and simulation with delay analysis which allows the design and validation of complex logic structures. The possibility to estimate the power consumption of the circuit.Microwind2 allows designing and simulating an integrated circuit at physical description level. The microwind contains a library of common logic and analog ICs to view and simulate. Circuit Simulation is done by pressing a single key. The electric extraction of the circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

4.1 Analysis of delay elements

4.1.1 Buffer

The figure shows the buffer which is replaced as a delay element with an inverter as in [4]. The purpose of the inverter here is to synchronous the speed of the NAND and NOR gate. And the layout created by the logic circuit is shown below where the power consumed by the circuit is 2.392mW and the crosstalk in the circuit is 0.02fF very low compared to other schemes.

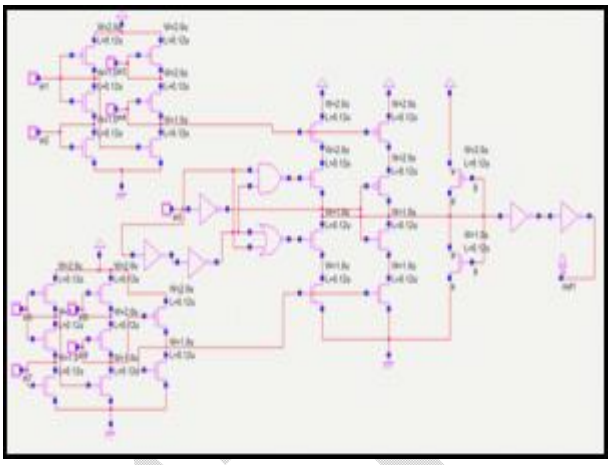

Fig 5: Circuit with buffer as a delay element

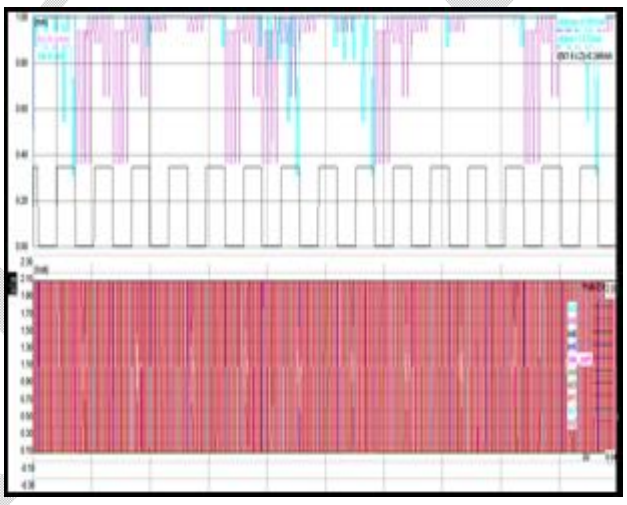

Fig 6: Output waveform voltage Vs current

4.1.2 D-Latch

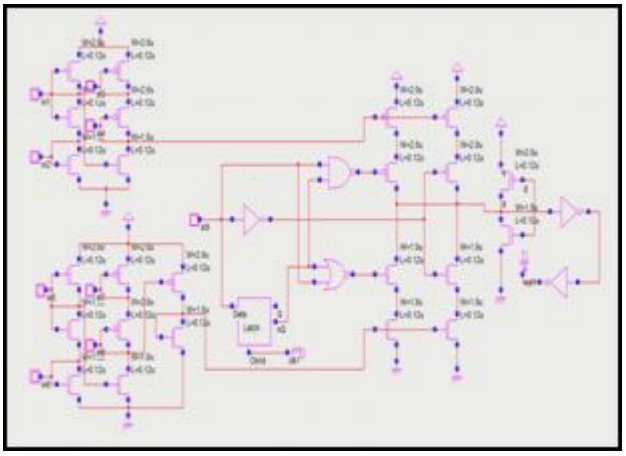

Fig 7: D-latch act as a delay element

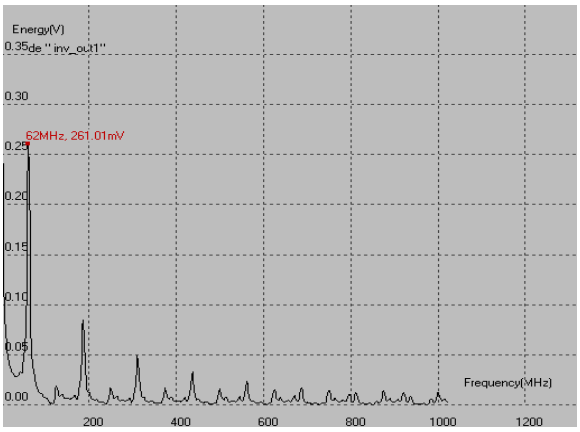

Fig 8: Output waveform voltage Vs current

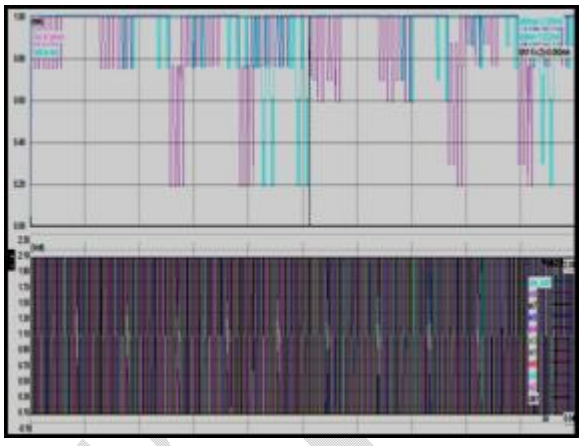

Fig 9:FFT calculation Frequency Vs Energy

4.1.3 Result analysis

Table.1

PERFORMANCE OF CMS—BIAS SCHEME WITH VARIOUS DELAY ELEMENT

SCHEMES	POWER (mW)	DELAY (ns)	ENERGY (KHz/mV)	ROUTED WIRES	I_{DDMAx} (mA)	I_{DDAVG} (mA)
CMS-BIAS with buffer	3.5	0.064	31/352.24	68	4.59	1.679
CMS-BIAS with D-Latch	3.4	0.061	62/261.01	65	3.365	1.522
CMS-BIAS with serial inverters	2.6	0.083	40000/491.88	61	2.939	1.301

4.1.4 Need of Current Mode Signaling

Current-Mode Signaling can be used to provide higher interconnect bandwidth when compared to traditional full-swing voltage-mode signaling, at the expense of increased DC power dissipation. Current-mode (CM) signaling is easier to implement with driver pre-emphasis technique because its logic states are determined by current values instead of voltage levels.

In reduced swing voltage mode signaling, the line is not terminated in low impedance as in [1]. Current mode signaling terminates the line in low impedance [1]. This reduces the time constant, increases bandwidth. However, this also leads to the static power consumption as in [5].

VI. CONCLUSION

Using CMS Scheme with bias circuit has a fine power consumption using d-latch and connection of serial buffers than the buffer. Reason is the complexity design of delay elements. By the application in On-Chip interconnection the process variation in supply, noise and temperature is controlled.

V. FUTURE WORK TO BE DONE

The sizing of the buffer can be varied and can be implemented in traffic light controller NETLIST and the Performance can be monitored in H-SPICE where the power is consumed. Otherwise the modification of the bias circuit and improvement in CMS-BIAS will give the speed and power improvement.

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